

## Issue:

**Complete RFIC Design Flow Targeting Next Generation Wireless Front-ends**

Besides the circuit design itself, a complete design flow based on a prescribed methodology is crucial for a successful implementation of next generation wireless front-ends. An integral part of this process is a scalable front-to-back solution that not only facilitates the job of the RFIC designer from the beginning, but also can be integrated with other domains such as analog/mixed-signal (AMS), digital and system design.

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The demand on mobile communications has grown over recent years. Today's mobile communication systems use sophisticated signal processing to achieve high transmission rates. The challenges for the next generation wireless systems will increase even further, when designs will need to meet multi-standards and achieve reconfigurability. Evaluations of various integration strategies will need to be performed to verify the feasibility of the proposed integration approach, where issues such as performance, cost and risk need to be considered. The requirements of the varying communication standards differ over a very wide range in terms of center frequency, signal bandwidth, signal-to-noise ratio, linearity, etc. This will have an impact on all radio front-end building blocks, and require comprehensive trade-off analysis to select the best appropriate architecture and derive the individual circuit block requirements.



Fig. 1 Block diagram of a dual-mode transceiver IC from Helic.

The complexity of digital signal processing is also steadily growing, as can be seen from the block diagram of a dual-band transceiver IC shown in *Figure 1*. The digital blocks offer the capability to compensate for some of the signal impairments caused by analog front-end blocks. To verify the complicated digital compensation algorithms, and the effect of analog nonidealities such as phase noise, nonlinearity and mismatch, the analog and digital blocks need to be simulated together. A key bottleneck to enable RF/baseband co-design is the presence of the RF carrier signal at several gigahertz in the RF front-end. To simulate the bit-error-rate (BER) or package-error-rate (PER) of a complete telecom link at the transistor-level and running thousands of cycles of the modulated signal is, at the very least, very expensive and often impractical.